IN THE CLAIMS

1.(amended) A record carrier having a signal recorded in a track, the signal comprising a sequence of successive information signal portions, each information signal portion representing an information word, wherein:

each of the information signal portions comprise n bit cells having a first or second signal value, ~~[and wherein]~~

a plurality of track information patterns represent the signal portions, ~~[characterized in that]~~

the information signal portions are spread over at least one group of a first type and at least one group of a second type, ~~[while]~~

each information signal portion belonging to a group of the first type uniquely represents an information word, ~~[and]~~

each information signal portion belonging to a group of the second type in combination with ~~[the]~~ logical ~~[signal]~~ values of p bit cells at predetermined positions in a following ~~[information]~~ signal portion represent a unique information word,

the logical values of bit cells of a signal portion being determinable from the signal values of that signal portion,

the signal portions including sync signal portions for synchronizing processing of the signal and having bit cell patterns that do not occur in the sequence of successive information signal portions,

for each information portion belonging to the at least one group of the second type, the following signal portion is in some cases an adjacent information signal portion and in other cases an adjacent sync signal portion,

thereby allowing one information signal portion belonging to the at least one ~~[a]~~ group of the second type to represent a plurality of information words among which the ~~respective~~ unique information word is distinguishable ~~[by the signal values]~~.

2.(amended) The record carrier as claimed in claim 1, characterized in that each number of successive bit cells having a same signal

value ranges from a minimum of d+1 to a maximum of k+1, and at any arbitrary point in the signal the running value of the difference between the number of bit cells having the first signal value and the bit cells having the second signal value in the signal ~~portion~~ preceding this point is [~~limited~~] kept low.

3. The record carrier as claimed in claim 2, characterized in that n is equal to 16, d is equal to 2 and k is equal to 10.

Cancel claims 4 and 5.

6.(amended) The record carrier as claimed in claim 2, characterized in that the information signal portions from the at least one group of the first type end in s bit cells having a [~~first~~] same logical [~~signal~~] value, and in that the information signal portions from the at least one group of the second type end in t bit cells having ~~a~~ the same logical [~~second signal~~]value, wherein s and t can assume different values and ~~wherein~~ the values that s [~~and t~~] can assume are all different than the values that t can assume [~~in value~~].

7.(amended) The record carrier as claimed in claim 2, wherein the track information patterns comprise first and second parts alternating in the direction of the track, the first parts presenting detectable first properties and the second parts presenting second properties distinguishable from the first properties, and wherein the parts having the first properties represent [~~bit cells having~~] the first signal value and the parts having the second properties represent [~~the bit cells having~~] the second signal value.

Cancel claim 8-9.

10.(amended) The record carrier as claimed in claim [~~8~~] 1, wherein the track information patterns comprise first and second parts alternating in the direction of the track, the first parts presenting detectable first properties and the second parts

presenting detectable second properties distinguishable from the first properties, and wherein the parts having the first properties represent [~~bit cells having~~] the first signal value and the parts having the second properties represent [~~the bit cells having~~] the second signal value.

11. The record carrier as claimed in claim 1, characterized in that p is equal to 2.

12.(amended) The record carrier as claimed in claim 1, characterized in that the information signal portions from the at least one group of the first type end in s bit cells having a [~~first~~] same logical [~~signal~~] value, and in that the information signal portions from the at least one group of the second type end in t bit cells having ~~a~~ the same [~~second signal~~] logical value, wherein s and t can assume different values and ~~wherein~~ the values that s ~~and t~~ can assume are all different than the values that t can assume ~~in value~~.

13.(amended) A [~~The~~] record carrier [~~as claimed in claim 12, characterized~~] having a signal recorded in a track, the signal comprising a sequence of successive signal portions including information signal portions,

each information signal portion representing an information word

each of the information signal portions includes n bit cells having a first or second signal value,

a plurality of track information patterns represent the signal portions,

the information signal portions are spread over at least one group of a first type and at least one group of a second type,

each information signal portion belonging to a group of the first type uniquely represents an information word,

each information signal portion belonging to a group of the second type in combination with the logical values of p bit cells at predetermined positions in a following information signal

portion represent a unique information word,

the logical values of a signal portion being determinable from the signal values of that signal portion,

thereby allowing one information signal portion belonging to the at least one group of the second type to represent a plurality of information words among which the unique information word is distinguishable, and

the information signal portions from the at least one group of the first type end in s bit cells having a same logical value, the information signal portions from the at least one group of the second type end in t bit cells having the same logical value, wherein s and t can assume different values and the values that s can assume are all different than the values that t can assume, and in that t is greater than or equal to 2 and smaller than or equal to 5.

14. (amended) The record carrier as claimed in claim [12] 13, wherein the track information patterns comprise first and second parts alternating in the direction of the track, the first parts presenting detectable first properties and the second parts presenting second properties distinguishable from the first properties, and wherein the parts having the first properties represent [bit cells having] the first signal value and the parts having the second properties represent [the bit cells having] the second signal value.

15. (amended) The record carrier as claimed in claim 1, wherein the track information patterns comprise first and second parts alternating in the direction of the track, the first parts presenting detectable first properties and the second parts presenting second properties distinguishable from the first properties, and wherein the parts having the first properties represent [bit cells having] the first signal value and the parts having the second properties represent [the bit cells having] the second signal value.

s

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16. The record carrier as claimed in claim 15, wherein said properties are optically detectable.

Please add the following new claims:

17. (new) The carrier of claim 13, in which the value of s is one of: 0-1 and 6-9.

18. (new) The carrier of claim 13, in which the presence or absence of changes of the signal value between the first and the second signal value represents the first or second logical value, and each number of successive bit cells having a same signal value ranges from a minimum of d+1 to a maximum of k+1.

19. (new) The carrier of claim 18, in which n is equal to 16, d is equal to 2 and k is equal to 10.

20. (new) The carrier of claim 13, in which the at least one group of the first type substantially comprises only information signal portions having logical values selected from:
0000000001000001, 0000000001000010, 0000000001001001,
0000000010000001, 0000000010000010, 0000000010001001,
0000000010010001, 0000000010010010, 0000000100000001,
0000000100000010, 0000000100001001, 0000000100010001,
0000000100010010, 0000000100100001, 0000000100100010,
0000001000000001, 0000001000000010, 0000001000001001,
0000001000010001, 0000001000010010, 0000001000100001,
0000001000100010, 0000001001000000, 0000001001000001,
0000001001000010, 0000001001001001, 0000010000000001,
0000010000000010, 0000010000001001, 0000010000010001,
0000010000010010, 0000010000100001, 0000010000100010,
0000010001000000, 0000010001000001, 0000010001000010,
0000010001001001, 0000010010000000, 0000010010000001,
0000010010000010, 0000010010001001, 0000010010010001,
0000010010010010, 0000010000000010, 0000100000001001,
0000100000010001, 0000100000010010, 0000100000100001,

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0000100000100010, 0000100001000000, 0000100001000001,
0000100001000010, 0000100001001001, 0000100010000000,
0000100010000001, 0000100010000010, 0000100010001001,
0000100010010001, 0000100010010010, 0000100100000000,
0000100100000001, 0000100100000010, 0000100100001001,
0000100100010001, 0000100100010010, 0000100100100001,
0000100100100010, 0001000000001001, 0001000000010001,
0001000000010010, 0001000000100001, 0001000000100010,
0001000001000000, 0001000001000001, 0001000001000010,
0001000001001001, 0001000010000000, 0001000010000001,
0001000010000010, 0001000010001001, 0001000010010001,
0001000010010010, 0001000100000000, 0001000100000001,
0001000100000010, 0001000100001001, 0001000100010001,
0001000100010010, 0001000100100001, 0001000100100010,
0001001000000000, 0001001000000001, 0001001000000010,
0001001000001001, 0001001000010001, 0001001000010010,
0001001000100001, 0001001000100010, 0001001001000000,
0001001001000001, 0001001001000010, 0001001001001001,
0010000000001001, 0010000000010001, 0010000000010010,
0010000000100001, 0010000000100010, 0010000001000000,
0010000001000001, 0010000001000010, 0010000001001001,
0010000010000000, 0010000010000001, 0010000010000010,
0010000010001001, 0010000010010001, 0010000010010010,
0010000100000000, 0010000100000001, 0010000100000010,
0010000100001001, 0010000100010001, 0010000100010010,
0010000100100001, 0010000100100010, 0010001000000000,
0010001000000001, 0010001000000010, 0010001000001001,
0010001000010001, 0010001000010010, 0010001000100001,
0010001000100010, 0010001001000000, 0010001001000001,
0010001001000010, 0010001001001001, 0010010000000001,
0010010000000010, 0010010000001001, 0010010000010001,
0010010000010010, 0010010000100001, 0010010000100010,
0010010001000000, 0010010001000001, 0010010001000010,
0010010001001001, 0010010010000000, 0010010010000001,
0010010010000010, 0010010010001001, 0010010010010001,
0010010010010010, 0100000000010001, 0100000000010010,

0100000000100001, 0100000000100010, 0100000001000000,
0100000001000001, 0100000001000010, 0100000001001001,
0100000010000000, 0100000010000001, 0100000010000010,
0100000010001001, 0100000010010001, 0100000010010010,
0100000100000000, 0100000100000001, 0100000100000010,
0100000100001001, 0100000100010001, 0100000100010010,
0100000100100001, 0100000100100010, 0100001000000000,
0100001000000001, 0100001000000010, 0100001000001001,
0100001000010001, 0100001000010010, 0100001000100001,
0100001000100010, 0100001001000000, 0100001001000001,
0100001001000010, 0100001001001001, 0100010000000001,
0100010000000010, 0100010000001001, 0100010000010001,
0100010000010010, 0100010000100001, 0100010000100010,
0100010001000000, 0100010001000001, 0100010001000010,
0100010001001001, 0100010010000000, 0100010010000001,
0100010010000010, 0100010010001001, 0100010010010001,
0100010010010010, 0100100000000010, 0100100000001001,
0100100000010001, 0100100000010010, 0100100000100001,
0100100000100010, 0100100001000001, 0100100001000010,
0100100001001001, 0100100010010001, 0100100010010010,
0100100100000000, 0100100100000001, 0100100100000010,
0100100100001001, 0100100100010001, 0100100100010010,
0100100100100001, 0100100100100010, 1000000000010001,
1000000000010010, 1000000000100001, 1000000000100010,
1000000001000000, 1000000001000001, 1000000001000010,
1000000001001001, 1000000010000000, 1000000010000001,
1000000010000010, 1000000010001001, 1000000010010001,
1000000010010010, 1000000100000000, 1000000100000001,
1000000100000010, 1000000100001001, 1000000100010001,
1000000100010010, 1000000100100001, 1000000100100010,
1000001000000000, 1000001000000001, 1000001000000010,
1000001000001001, 1000001000010001, 1000001000010010,
1000001000100001, 1000001000100010, 1000001001000000,
1000001001000001, 1000001001000010, 1000001001001001,
1000010000000001, 1000010000000010, 1000010000001001,

1000010000010001, 1000010000010010, 1000010000100001, 1000010000100010, 1000010001000000, 1000010001000001, 1000010001000010, 1000010001001001, 1000010010000000, 1000010010000001, 1000010010000010, 1000010010001001, 1000010010010001, 1000010010010010, 1000100000000010, 1000100000001001, 1000100000010001, 1000100000010010, 1000100000100001, 1000100000100010, 1000100001000000, 1000100001000001, 1000100001000010, 1000100001001001, 1000100010000000, 1000100010000001, 1000100010000010, 1000100010001001, 1000100010010001, 1000100010010010, 1000100100000000, 1000100100000001, 1000100100000010, 1000100100001001, 1000100100010001, 1000100100010010, 1000100100100001, 1000100100100010, 1001000000001001, 1001000000010001, 1001000000010010, 1001000000100001, 1001000000100010, 1001000001000000, 1001000001000001, 1001000001000010, 1001000001001001, 1001000010000000, 1001000010000001, 1001000010000010, 1001000010001001, 1001000010010001, 1001000010010010, 1001000100000000, 1001000100000001, 1001000100000010, 1001000100001001, 1001000100010001, 1001000100010010, 1001000100100001, 1001000100100010, 1001001000000000, 1001001000000001, 1001001000000010, 1001001000001001, 1001001000010001, 1001001000010010, 1001001000100001, 1001001000100010, 1001001001000000, 1001001001000001, 1001001001000010, 1001001001001001,

where "0" represents a first logical value and where "1" represents a second logical value.

21. (new) The carrier of claim 20, in which the at least one group of the second type substantially comprises only information signal portions having logical values selected from:

0000000001000100, 0000000001001000, 0000000010000100, 0000000010001000, 0000000010010000, 0000000100000100, 0000000100001000, 0000000100010000, 0000000100100000, 0000000100100100, 0000001000000100, 0000001000001000,

0000001000010000, 0000001000100000, 0000001000100100,
0000001001000100, 0000001001001000, 0000010000000100,
0000010000001000, 0000010000010000, 0000010000100000,
0000010000100100, 0000010001000100, 0000010001001000,
0000010010000100, 0000010010001000, 0000010010010000,
0000100000000100, 0000100000001000, 0000100000010000,
0000100000100000, 0000100000100100, 0000100001000100,
0000100001001000, 0000100010000100, 0000100010001000,
0000100010010000, 0000100100000100, 0000100100001000,
0000100100010000, 0000100100100000, 0000100100100100,
0001000000000100, 0001000000001000, 0001000000010000,
0001000000100000, 0001000000100100, 0001000001000100,
0001000001001000, 0001000010000100, 0001000010001000,
0001000010010000, 0001000100000100, 0001000100001000,
0001000100010000, 0001000100100000, 0001000100100100,
0001001000000100, 0001001000001000, 0001001000010000,
0001001000100000, 0001001000100100, 0001001001000100,
0001001001001000, 0010000000001000, 0010000000010000,
0010000000100000, 0010000000100100, 0010000001000100,
0010000001001000, 0010000010000100, 0010000010001000,
0010000010010000, 0010000100000100, 0010000100001000,
0010000100010000, 0010000100100000, 0010000100100100,
0010001000000100, 0010001000001000, 0010001000010000,
0010001000100000, 0010001000100100, 0010001001000100,
0010001001001000, 0010010000000100, 0010010000001000,
0010010000010000, 0010010000100000, 0010010000100100,
0010010001000100, 0010010001001000, 0010010010000100,
0010010010001000, 0010010010010000, 0100000000010000,
0100000000100000, 0100000000100100, 0100000001000100,
0100000001001000, 0100000010000100, 0100000010001000,
0100000010010000, 0100000100000100, 0100000100001000,
0100000100010000, 0100000100100000, 0100000100100100,
0100001000000100, 0100001000001000, 0100001000010000,
0100001000100000, 0100001000100100, 0100001001000100,
0100001001001000, 0100010000000100, 0100010000001000,
0100010000010000, 0100010000100000, 0100010000100100,

0100010001000100, 0100010001001000, 0100010010000100,
0100010010001000, 0100010010010000, 0100100000000100,
0100100000001000, 0100100000010000, 0100100000100000,
0100100000100100, 0100100001000100, 0100100001001000,
0100100010000100, 0100100010001000, 0100100010010000,
0100100100000100, 0100100100001000, 0100100100010000,
0100100100100000, 0100100100100100, 1000000000100000,
1000000000100100, 1000000001000100, 1000000001001000,
1000000010000100, 1000000010001000, 1000000010010000,
1000000100000100, 1000000100001000, 1000000100010000,
1000000100100000, 1000000100100100, 1000001000000100,
1000001000001000, 1000001000010000, 1000001000100000,
1000001000100100, 1000001001000100, 1000001001001000,
1000010000000100, 1000010000001000, 1000010000010000,
1000010000100000, 1000010000100100, 1000010001000100,
1000010001001000, 1000010010000100, 1000010010001000,
1000010010010000, 1000100000000100, 1000100000001000,
1000100000010000, 1000100000100000, 1000100000100100,
1000100001000100, 1000100001001000, 1000100010000100,
1000100010001000, 1000100010010000, 1000100100000100,
1000100100001000, 1000100100010000, 1000100100100000,
1000100100100100, 1001000000000100, 1001000000001000,
1001000000010000, 1001000000100000, 1001000000100100,
1001000001000100, 1001000001001000, 1001000010000100,
1001000010001000, 1001000010010000, 1001000100000100,
1001000100001000, 1001000100010000, 1001000100100000,
1001000100100100, 1001001000000100, 1001001000001000,
1001001000010000, 1001001000100000, 1001001000100100,
1001001001000100, 1001001001001000,

where "0" represents a first logical value and where "1" represents a second logical value.

22. (new) A method of converting a series of m-bit information words to a modulated signal, with m being an integer, in which method an n-bit code word is delivered for each received information word, with n being an integer exceeding m, and the

delivered code words are converted to the modulated signal, and in which the series of information words is converted to a series of code words according to rules of conversion so that the corresponding modulated signal satisfies a predetermined criterion, in which the code words are organizable into at least one group of code words of a first type and at least one group of code words of a second type, where the delivery of each of the code words belonging to a group of the first type establishes a first type of coding state determined only by the group to which that code word belongs, and the delivery of each of the code words belonging to a group of the second type establishes a second type of coding state determined not only by the group to which that code word belongs but also by information content in the information word itself for which that code word is delivered, all the code words that establish the same state belonging to the same group, some code words belonging to more than one group, each state corresponding to one of the groups, groups of the first type corresponding to one state of the first type and groups of the second type corresponding to more than one state of the second type, each coding state corresponding to a different set of code words into which information words are converted and when one of the code words is assigned to a received information word, that code word is selected from the set of code words that corresponds to the coding state of the first type or the second type established when a preceding code word was delivered, where the sets of code words corresponding to respective coding states of the second type are sets of the second type, there are multiple sets of the second type and each set of the second type does not contain any code words in common with other sets of the second type, in which at least one of the sets of code words for each of at least a number of information words comprise at least a pair of code words, with low-frequency components in the modulated signal being repressed when the information words are converted by selection of code words from the pairs of code words.

23. (new) A method of converting a series of m-bit information

words to a modulated signal, with m being an integer, in which method an n-bit code word is delivered for each received information word, with n being an integer exceeding m, and the delivered code words are converted to the modulated signal, and in which the series of information words is converted to a series of code words according to rules of conversion so that the corresponding modulated signal satisfies a predetermined criterion, in which the code words are organizable into at least one group of code words of a first type and at least one group of code words of a second type, where the delivery of each of the code words belonging to a group of the first type establishes a first type of coding state determined only by the group to which that code word belongs, and the delivery of each of the code words belonging to a group of the second type establishes a second type of coding state determined not only by the group to which that code word belongs but also by information content in the information word itself for which that code word is delivered, each coding state corresponding to a different set of code words into which information words are converted and when one of the code words is assigned to a received information word, that code word is selected from the set of code words that corresponds to the coding state of the first type or the second type established when a preceding code word was delivered, where code words contained in different sets corresponding with respective coding states of the second type do not contain any code words in common with other sets, in which code words contained in different sets associated with the coding states of the second type are mutually distinguishable on the basis of the logical values of bits at p predetermined non-consecutive bit positions in the code words, where p is an integer smaller than n, and in which low frequency components of the modulated signal are repressed.

24. (new) The method of claim 22, in which a running digital sum value is established as a measure for current DC contents, which value is determined over a preceding portion of the modulated signal and denotes for this portion the current value of a difference between the number of bit cells having a first signal

value and the number of bit cells having a second signal value, the pairs of code words comprising two code words having opposite effects on the digital sum value, and the code words are selected from the pairs in response to certain digital sum values so that the digital sum value is kept low.

25. (new) The method of claim 22, in which the modulated signal has bit cells of a first signal value and bit cells of a second signal value, and the series of information words are converted to a series of code words which establish a bit string having bits of a first logical value and bits of a second logical value, in which a number of successive bits having the first logical value and situated among bits having the second logical value is at least d and at most k, and the bit string is converted to the modulated signal, in which transitions from bit cells having the first signal value to bit cells having the second signal value or vice versa correspond to the bits having the second logical value in the bit string.

26. (new) The method of claim 22, in which the code words are made up of bits having first and second logical values, and code words contained in different sets associated with the coding states of the second type are mutually distinguishable on the basis of the logical values of bits at p predetermined non-consecutive bit positions in the code words, where p is an integer smaller than n

27. (new) The method of claim 26, in which sync words are inserted into the series of code words, the sync words showing bit patterns that cannot occur in a bit string formed by the code words and having different bit patterns, the sync word being used depends on the coding state prior to its insertion, and it establishes a predetermined coding state for the conversion of the next information word to be converted after its insertion, and the sync words being mutually distinguishable on the basis of the logical values of bits at predetermined bit positions in a manner corresponding to the manner in which the code word sets

corresponding to coding states of the second type are mutually distinguishable from each other.

28. (new) The method of claim 26, in which p is equal to 2.

29. (new) The method of claim 22, in which d is equal to 2, k is equal to 10 and the ratio of n to m is 2:1.

30. (new) The method of claim 29, in which m is equal to 8, and n is equal to 16.

31. (new) The method of claim 28, in which the code words are made up of bits having a first logical value and bits having a second logical value, a first group of the first type of code words is formed by code words ending in a bits having the first logical value, where a is equal to 0 or 1, a second group of the first type of code words is formed by code words ending in b successive bits having the first logical value, where b is an integer greater than or equal to 6 and smaller than or equal to 9, a group of the second type is formed by code words ending in c successive bits having the first logical value, where c is an integer greater than or equal to 2 and smaller than or equal to 5, and the coding state related sets of code words from which the code words assigned to the information words are selected are formed by code words beginning with a number of bits of the first logical value, which number of bits depends on the coding state related to the set, so that the number of successive bits having the first logical value in a bit string formed by two successive code words is at least equal to d and at most equal to k.

32. (new) A method for manufacturing a record carrier in which a modulated signal is generated by the method of claim 22 and the record carrier is then provided with an information pattern representing this signal.

33. (new) An encoding device, comprising an m-to-n bit converter

for converting m-bit information words to n-bit code words, means for converting the n-bit code words to a modulated signal, and state establishing means for establishing a coding state on the delivery of a code word by the converter, the state establishing means being arranged for establishing a first type of coding state for each delivered code word belonging to a group of a first type, which state is determined only by the group to which the delivered code word belongs, and for establishing a second type of coding state for each of the delivered code words belonging to a group of the second type, which state is determined not only by the group to which the delivered code word belongs but also by information content in the information word converted into the delivered code word, in which the m-to-n bit converter comprises means for selecting a code word corresponding to an information word from a set of code words corresponding respectively to the established coding state of the first type or the second type, sets of code words corresponding to respective coding states of the second type containing no code words in common with other sets of code words corresponding to respective coding states of the second type, in which the code words are made up of bits having first and second logical values and code words contained in different sets associated with the coding states of the second type are mutually distinguishable on the basis of the logical values of bits at p predetermined non-consecutive bit positions in the code words, where p is an integer smaller than n, and in which low frequency components of the modulated signal are repressed.

34. (new) An encoding device, comprising an m-to-n bit converter for converting m-bit information words to n-bit code words, means for converting the n-bit code words to a modulated signal, and state establishing means for establishing a coding state on the delivery of a code word by the converter, the state establishing means being arranged for establishing a first type of coding state for each delivered code word belonging to a group of a first type, which state is determined by the group from which the delivered code word belongs, and for establishing a second type of coding

state for each of the delivered code words belonging to a group of the second type, which state is determined by the information word which is to be converted to the delivered code word, in which the m-to-n bit converter comprises means for selecting a code word corresponding to an information word from a set of code words that depends on the coding state of the first type or the second type established, all the code words that establish the same state belonging to the same group, some code words belonging to more than one group, each state corresponding to one of the groups, groups of the first type corresponding to one state of the first type and groups of the second type corresponding to more than one state of the second type, sets of code words corresponding respectively to coding states of the second type contain no code words in common with other sets of code words corresponding respectively to coding states of the second type, the modulated signal having bit cells and presenting substantially no frequency components in a low-frequency area in the frequency spectrum, in which each minimum number of successive bit cells having the same signal value is d+1 and each maximum number k+1, the converter further comprises means for generating a pair of code words for each of at least a number of information words, and the device further comprises selecting means for selecting, for the code word delivery, either of the code words from the pairs in accordance with a predetermined criterion related to the low-frequency contents of the modulated signal.

35. (new) The device of claim 34, further comprising means for determining a running digital sum value, which value denotes for a preceding part of the modulated signal the running value of a difference between the number of bit cells having a first signal value and the number of bit cells having a second signal value, in which the pairs of code words comprising each at least two code words have opposite effects on the digital sum value, and the selecting means comprises means for selecting, according to a criterion depending on the digital sum value, those code words from the sets for which the digital sum value according to this criterion continues to be kept low.

36. (new) The device of claim 34, in which the device is arranged for converting the information words to a series of code words which establish a bit string of bits having a first logical value and bits having a second logical value, the minimum number of successive bits having the first logical value located between bits having the second logical value being d and the maximum number being k, and the device further comprises a modulo-2 integrator for converting the bit string to the modulated signal.

37. (new) The device of claim 34, in which the code words contained in different sets associated with the coding states of the second type are mutually distinguishable on the basis of the logical values of bits at p predetermined non-consecutive bit positions in the code words, where p is an integer smaller than n

38. (new) The device of claim 37, further comprising means for inserting sync words into a bit string formed by the code words, the sync words displaying bit patterns that cannot occur in the bit string formed by the code words, means for selecting sync words to be inserted which have different bit patterns depending on the determined coding state, the sync words being mutually distinguishable on the basis of the logical values of bits at predetermined non-consecutive bit positions in a manner that corresponds to a manner in which the code words in the code word sets corresponding respectively to the coding states of the second type, can be mutually distinguished.

39. (new) The device of claim 38, further comprising means for effecting a predetermined coding state once a sync word has been inserted.

40. (new) The device of claim 37, in which p is equal to 2.

41. (new) The device of claim 34, in which d is equal to 2, k is equal to 10, and the ratio of n to m is 2:1.

42. (new) The device of claim 41, in which m is equal to 8, and n is equal to 16.

43. (new) The device of claim 41, in which the code words are made up of bits having a first logical value and bits having a second logical value, a first group of the first type of code words is formed by code words ending in a bits having the first logical value, where a is equal to 0 or 1, a second group of the first type of code words is formed by code words ending in b successive bits having the first logical value, where b is an integer greater than or equal to 6 and smaller than or equal to 9, a group of the second type is formed by code words ending in c successive bits having the first logical value, where c is an integer greater than or equal to 2 and smaller than or equal to 5, and the coding state related sets of code words from which the code words assigned to the information words are selected are formed by code words beginning with a number of bits of the first logical value, which number of bits depends on the coding state related to the set, so that the number of successive bits having the first logical value in a bit string formed by two successive code words is at least equal to d and at most equal to k.

44. (new) A device for recording information, which device comprises a coding device of claim 34 for converting a series of information words representing the information to a modulated signal, and means for recording on a record carrier an information pattern corresponding to the signal.

45. (new) A modulated signal representing a series of information words for subsequent demodulation and decoding to reproduce the represented series of information words, the coded signal comprising a sequence of q successive information signal portions which represent q information words, where q is an integer, in which signal each of the information signal portions represents one of the information words and comprises n bit cells, each the bit

cell having a first or second logical value, each information signal portion belonging to one of a plurality of predetermined groups of information signal portions, each information signal portion belonging to a first one of the groups of information signal portions uniquely establishing an information word irrespective of information signal portions adjacent to the each information signal portion belonging to the first group, and each information signal portion belonging to a second one of the groups of information signal portions uniquely establishing an information word depending upon the logical value of p predetermined non-consecutive bit cells in an information signal portion adjacent to the each information signal portion belonging to the second group, where p is an integer smaller than n, and in which low frequency components of the modulated signal are repressed.

46. (new) The signal of claim 45, in which the presence or absence of changes of the signal value between a first and a second signal value represents the first or second logical value, each number of successive bit cells having the same signal value is minimum d+1 and maximum k+1, and at any arbitrary point in the signal, the running value of the difference between the number of bit cells having the first signal value and the number of bit cells having the second signal value in a signal portion preceding that point is kept low.

47. (new) The signal of claim 46, in which n is equal to 16, d is equal to 2, and k is equal to 10.

48. (new) A modulated signal representing a series of information words for subsequent demodulation and decoding to reproduce the represented series of information words, the coded signal comprising:

a sequence of q successive information signal portions which represent q information words, where q is an integer, and

sync signal portions which have bit cell patterns that do not occur in the sequence of successive information signal portions;

and in which signal:

each of the information signal portions represents one of the information words and comprises n bit cells,

each the bit cell having a first or second signal property,

each information signal portion belonging to one of a plurality of predetermined groups of information signal portions,

each information signal portion belonging to a first one of the groups of information signal portions uniquely establishing an information word irrespective of information signal portions adjacent to the each information signal portion belonging to the first group,

each information signal portion belonging to a second one of the groups of information signal portions uniquely establishing an information word depending upon the value of at least one bit cell in a signal portion adjacent to the each information signal portion belonging to the second group, the adjacent signal portion containing the at least one bit cell are in some cases an adjacent information signal portion and in other case are an adjacent sync signal portion.

49. (new) The signal of claim 48, in which the presence or absence of changes of the signal value between a first and a second signal value represents the first or second logical value.

50. (new) The signal of claim 49, in which p is equal to 2.

51. (new) The signal of claim 45, in which the information signal portions from the first group end in s bit cells having a same logical value, and the information signal portions from the second group end in t bit cells having the same logical value, wherein s and t can each assume a number of different values and the values that s can assume are all different than the values that t can assume.

52. (new) The signal of claim 51, in which t is greater than or equal to 2, and smaller than or equal to 5.

53. (new) A record carrier on which the signal of claim 45 is stored in a track in which information patterns represent the signal portions, which information patterns comprise first and second parts alternating in the direction of the track, the first parts present detectable first properties and the second parts present second properties distinguishable from the first properties, and the presence or absence of changes between the parts having the first properties and the parts having the second properties represents the first or second logical value.

54. (new) A decoding device for converting a modulated signal to a series of m-bit information words, the device comprising:

demodulation means for converting the modulated signal to a bit string of bits having a first or second logical value, which bit string contains a series of n-bit code words which correspond to the information signal portions, and

converting means for converting the series of code words to the series of information words, an information word being assigned to each of the code words to be converted and depending thereon, in which the converting means convert a code word to an information word also depending on the logical values of bits located at p predetermined non-consecutive positions in a portion of the bit string adjacent to the code word, where p is an integer smaller than n, and in which the converting means convert a code word selected from at least a pair of code words into an information word for each of at least a number of information words with low-frequency components in the signal being repressed by the selected code word.

55. (new) The device of claim 54, in which n is equal to 16, m is equal to 8, and p is equal to 2.

56. (new) The device of claim 55, in which the p predetermined bit positions are 12 bit positions apart.

57. (new) A decoding device for converting a coded signal modulated and stored on a record carrier to a series of m-bit information words, the coded signal representing a series of information words for subsequent reading, demodulation and decoding to reproduce the represented series of information words, the coded signal comprising:

a sequence of q successive information signal portions which represent q information words, where q is an integer, in which signal each of the information signal portions represents one of the information words and comprises n bit cells, each the bit cell having a first or second signal property,

each information signal portion belonging to one of a plurality of predetermined groups of information signal portions,

each information signal portion belonging to a first one of the groups of information signal portions uniquely establishing an information word irrespective of information signal portions adjacent to the each information signal portion belonging to the first group, and

each information signal portion belonging to a second one of the groups of information signal portions uniquely establishing an information word depending upon the value of at least one bit cell in an information signal portion adjacent to the each information signal portion belonging to the second group,

the decoding device comprising:

means for converting the signal to a bit string of bits having a first or second logical value, which bit string contains sync words and a series of n-bit code words which correspond to the information signal portions,

converting means for converting the series of code words to the series of information words, an information word being assigned to each of the code words to be converted and depending thereon, in which the converting means convert a code word to an information word also depending on the logical values of bits in the bit string which are located at p predetermined positions relative to the code word, the bits being in some cases contained in another code word and in other cases contained in a sync word, and

detection means for detecting sync words, the sync words having bit patterns that cannot be formed by the successive code words in the series.

58. (new) The device of claim 57, in which the detection means detect 26-bit sync words corresponding to a bit pattern of "10010000000000100000000001" or to a bit pattern of "00010000000000100000000001", where "0" represents a first logical value and where "1" represents a second logical value.

59. (new) A reading device for reading a record carrier on which information is recorded in an information pattern, the device comprising:

means for converting the information pattern to a corresponding modulated signal, and

demodulation means for converting the modulated signal to a bit string of bits having a first or second logical value, which bit string contains a series of n-bit code words which correspond to the information signal portions, and

converting means for converting the series of code words to the series of information words, an information word being assigned to each of the code words to be converted and depending thereon, in which the converting means convert a code word to an information word also depending on the logical values of bits located at p predetermined non-consecutive positions in a portion of the bit string adjacent to the code word, where p is an integer smaller than n, and in which the converting means convert a code word selected from at least a pair of code words into an information word for each of at least a number of information words with low-frequency components in the signal being repressed by the selected code word.

60. (new) The method of Claim 26, in which the p predetermined bit positions are 12 bit positions apart.

61. (new) The method of Claim 23 in which the p predetermined bit

positions are 12 bit positions apart.

62. (new) The method of Claim 22, in which the at least a number of information words constitutes a lexicographically consecutive range smaller than the range of information words.

63. (new) The method of Claim 62, in which the lexicographically consecutive range is equal for all sets.

64. (new) The method of Claim 62, in which the lexicographically consecutive range ranges from information word 0 to information word 87.

65. (new) The device of Claim 33, in which the p predetermined bit positions are the first and thirteenth bit position.

66. (new) The device of Claim 40, in which the p predetermined bit positions are the first and thirteenth bit position.

67. (new) The device of Claim 33, in which the at least a number of information words constitutes a lexicographically consecutive range smaller than the range of information words.

68. (new) The method of Claim 67, in which the lexicographically consecutive range is equal for all sets

69. (new) The device of Claim 67, in which the lexicographically consecutive range ranges from information word 0 to information word 87.

70. (new) The carrier of Claim 41, in which the p predetermined bit positions are the first and thirteenth bit position.

71. (new) The carrier of Claim 41, in which the at least a number of information words constitutes a lexicographically consecutive range smaller than the range of information words.

72. (new) The carrier of Claim 71, in which the lexicographically consecutive range ranges from information word 0 to information word 87.

73. (new) The signal of Claim 46, in which the p predetermined bit positions are the first and thirteenth bit position.

74. (new) The signal of Claim 51, in which the p predetermined bit positions are the first and thirteenth bit position.

75. (new) The signal of Claim 46, in which the at least a number of information words constitutes a lexicographically consecutive range smaller than the range of information words.

76. (new) The signal of Claim 75, in which the lexicographically consecutive range ranges from information word 0 to information word 87.

77. (new) The device of Claim 54, in which the at least a number of information words constitutes a lexicographically consecutive range smaller than the range of information words.

78. (new) The device of Claim 77, in which the lexicographically consecutive range ranges from information word 0 to information word 87.

79. (new) The carrier of claim 2 in which the successive bit cells have the same signal value ranges from a minimum of d+1 to a maximum of k+1 both within information signal portions and across information signal portion boundaries.

80. (new) The carrier of claim 18 in which the successive bit cells have the same signal value ranges from a minimum of d+1 to a maximum of k+1 both within information signal portions and across information signal portion boundaries.

81. (new) The method of claim 25 in which the successive bit cells have the same signal value ranges from a minimum of d+1 to a maximum of k+1 both within information signal portions and across information signal portion boundaries.

82. (new) The method of claim 31 in which the successive bit cells have the same signal value ranges from a minimum of d+1 to a maximum of k+1 both within information signal portions and across information signal portion boundaries.

83. (new) The device of claim 34 in which the successive bit cells have the same signal value ranges from a minimum of d+1 to a maximum of k+1 both within information signal portions and across information signal portion boundaries.

84. (new) The device of claim 43 in which the successive bit cells have the same signal value ranges from a minimum of d+1 to a maximum of k+1 both within information signal portions and across information signal portion boundaries.

85. (new) The signal of claim 46 in which the successive bit cells have the same signal value ranges from a minimum of d+1 to a maximum of k+1 both within information signal portions and across information signal portion boundaries.

86. (new) A method of converting a series of m-bit information words to a modulated signal, with m being an integer, in which method an n-bit code word is delivered for each received information word, with n being an integer exceeding m, and the delivered code words are converted to the modulated signal, and in which the series of information words is converted to a series of code words according to rules of conversion so that the corresponding modulated signal satisfies a predetermined criterion, in which the code words are divided into at least one group of code words of a first type and at least one group of code words of a

second type, where the delivery of each of the code words belonging to a group of the first type establishes a first type of coding state determined only by the group to which that code word belongs, and the delivery of each of the code words belonging to a group of the second type establishes a second type of coding state determined not only by the group to which that code word belongs but also by information content in the information word itself for which that code word is delivered, each coding state corresponding to a different set of code words into which information words are converted and when one of the code words is assigned to a received information word, that code word is selected from the set of code words that corresponds to the coding state of the first type or the second type established when a preceding code word was delivered, where the sets of code words corresponding to coding states of the second type do not contain any code words in common, and in that the signal comprises sync signal portions which have bit cell patterns that do not occur in the sequence of successive information signal portions, while a unique information word is established by the information signal portions of the second group combined with an adjacent signal portion being in some cases an adjacent sync signal portion and in other cases an adjacent information signal portion.

87. (new) An encoding device, comprising an m-to-n bit converter for converting m-bit information words to n-bit code words, means for converting the n-bit code words to a modulated signal, and state establishing means for establishing a coding state on the delivery of a code word by the converter, the state establishing means being arranged for establishing a first type of coding state for each delivered code word belonging to a group of a first type, which state is determined only by the group to which the delivered code word belongs, and for establishing a second type of coding state for each of the delivered code words belonging to a group of the second type, which state is determined not only by the group to which the delivered code word belongs but also by information content in the information word converted into the delivered code

word, in which the m-to-n bit converter comprises means for selecting a code word corresponding to an information word from a set of code words, the set corresponding respectively to the established coding state of the first type or the second type , sets of code words corresponding respectively to coding states of the second type containing no code words in common with other sets of code words corresponding respectively to coding states of the second type, and in that the signal comprises sync signal portions which have bit cell patterns that do not occur in the sequence of successive information signal portions, while a unique information word is established by the information signal portions of the second group combined with an adjacent signal portion being in some cases an adjacent sync signal portion and in other cases an adjacent information signal portion.

88. (new) A device for recording information, which device comprises a coding device of claim 87 for converting a series of information words representing the information to a modulated signal, and means for recording on a record carrier an information pattern corresponding to the signal.

89. (new) A coded signal modulated and stored on a record carrier and representing a series of information words for subsequent reading, demodulation and decoding to reproduce the represented series of information words, the coded signal comprising a sequence of q successive information signal portions which represent q information words, where q is an integer, in which signal each of the information signal portions represents one of the information words and comprises n bit cells, each the bit cell having a first or second logical value, each information signal portion belonging to one of a plurality of predetermined groups of information signal portions, each information signal portion belonging to a first one of the groups of information signal portions uniquely establishing an information word irrespective of information signal portions adjacent to the each information signal portion belonging to the first group, and each information signal portion belonging to a

second one of the groups of information signal portions uniquely establishing an information word depending upon the information signal portion adjacent to the each information signal portion belonging to the second group, and in that the signal comprises sync signal portions which have bit cell patterns that do not occur in the sequence of successive information signal portions, while a unique information word is established by the information signal portions of the second group combined with an adjacent signal portion being in some cases an adjacent sync signal portion and in other cases an adjacent information signal portion.

90. (new) A decoding device for converting a modulated signal to a series of m-bit information words, the device comprising:
demodulation means for converting the modulated signal to a bit string of bits having a first or second logical value, which bit string contains a series of n-bit code words which correspond to information signal portions, and converting means for converting the series of code words to the series of information words, an information word being assigned to each of the code words to be converted and depending thereon, in which the converting means convert a code word to an information word also depending on another code word adjacent to the code word being converted, and in that the signal comprises sync signal portions which have bit cell patterns that do not occur in the sequence of successive information signal portions, while a unique information word is established by the information signal portions of the second group combined with an adjacent signal portion being in some cases an adjacent sync signal portion and in other cases an adjacent information signal portion.

91. (new) A reading device for reading a record carrier on which information is recorded in an information pattern, the device comprising:

reading means for converting the information pattern to a corresponding modulated signal,

demodulation means for converting the modulated signal to a

bit string of bits having a first or second logical value, which bit string contains a series of n-bit code words which correspond to the information signal portions, and

converting means for converting the series of code words to the series of information words, an information word being assigned to each of the code words to be converted and depending thereon, in which the converting means convert a code word to an information word also depending on another code word adjacent to the code word being converted, and in that the signal comprises sync signal portions which have bit cell patterns that do not occur in the sequence of successive information signal portions, while a unique information word is established by the information signal portions of the second group combined with an adjacent signal portion being in some cases an adjacent sync signal portion and in other cases an adjacent information signal portion.

92. (new) A method of converting a series of m-bit information words to a modulated signal, with m being an integer, in which method an n-bit code word is delivered for each received information word, with n being an integer exceeding m, and the delivered code words are converted to the modulated signal, and in which the series of information words is converted to a series of code words according to rules of conversion so that the corresponding modulated signal satisfies a predetermined criterion, in which the code words are organizable into at least one group of code words of a first type and at least one group of code words of a second type, where the delivery of each of the code words belonging to a group of the first type establishes a first type of coding state determined only by the group to which that code word belongs, and the delivery of each of the code words belonging to a group of the second type establishes a second type of coding state determined not only by the group to which that code word belongs but also by information content in the information word itself for which that code word is delivered, each coding state corresponding to a different set of code words into which information words are converted and when one of the code words is assigned to a received

information word, that code word is selected from the set of code words that corresponds to the coding state of the first type or the second type established when a preceding code word was delivered, where the sets of code words corresponding to coding states of the second type do not contain any code words in common, the information signal portions from the at least one group of the first type end in s bit cells having a same logical value, the information signal portions from the at least one group of the second type end in t bit cells having a same logical value, in which s and t can assume different values and the values that s can assume are different than all the values that t can assume, and t is greater than or equal to 2 and smaller than or equal to 5.

93. (new) An encoding device, comprising an m-to-n bit converter for converting m-bit information words to n-bit code words, means for converting the n-bit code words to a modulated signal, and state establishing means for establishing a coding state on the delivery of a code word by the converter, the state establishing means being arranged for establishing a first type of coding state for each delivered code word belonging to a group of a first type, which state is determined only by the group to which the delivered code word belongs, and for establishing a second type of coding state for each of the delivered code words belonging to a group of the second type, which state is determined not only by the group to which the delivered code word belongs but also by information content in the information word converted into the delivered code word, in which the m-to-n bit converter comprises means for selecting a code word corresponding to an information word from a set of code words belonging to the coding state of the first type or the second type established, sets of code words belonging to coding states of the second type containing no code words in common, the information signal portions from the at least one group of the first type end in s bit cells having a same logical value, the information signal portions from the at least one group of the second type end in t bit cells having a same logical value, in which s and t can assume different values and the values that s can

assume are different than all the values that t can assume, and t is greater than or equal to 2 and smaller than or equal to 5.

94. (new) A device for recording information, which device comprises a coding device of claim 93 for converting a series of information words representing the information to a modulated signal, and means for recording on a record carrier an information pattern corresponding to the signal.

95. (new) A coded signal modulated and stored on a record carrier and representing a series of information words for subsequent reading, demodulation and decoding to reproduce the represented series of information words, the coded signal comprising a sequence of q successive information signal portions which represent q information words, where q is an integer, in which signal each of the information signal portions represents one of the information words and comprises n bit cells, each the bit cell having a first or second logical value, each information signal portion belonging to one of a plurality of predetermined groups of information signal portions, each information signal portion belonging to a first one of the groups of information signal portions uniquely establishing an information word irrespective of information signal portions adjacent to the each information signal portion belonging to the first group, and each information signal portion belonging to a second one of the groups of information signal portions uniquely establishing an information word depending upon the information signal portion adjacent to the each information signal portion belonging to the second group, the information signal portions from the at least one group of the first type end in s bit cells having a same logical value, the information signal portions from the at least one group of the second type end in t bit cells having a same logical value, in which s and t can assume different values and the values that s can assume are different than all the values that t can assume, and t is greater than or equal to 2 and smaller than or equal to 5.

96. (new) A decoding device for converting a modulated signal to a series of m-bit information words, the device comprising:

demodulation means for converting the modulated signal to a bit string of bits having a first or second logical value, which bit string contains a series of n-bit code words which correspond to the information signal portions, and

converting means for converting the series of code words to the series of information words, an information word being assigned to each of the code words to be converted and depending thereon, in which the converting means convert a code word to an information word also depending on another portion of the bit stream adjacent to the code word being converted if the information signal portions end in t bit cells having a same logical value, and not if the information signal portions end in s bit cells having a same logical value, where s and t can assume different values, the values that s can assume are all different than the values that t can assume, and t is greater than or equal to 2 and smaller than or equal to 5.

97. (new) A reading device for reading a record carrier on which information is recorded in an information pattern, the device comprising:

reading means for converting the information pattern to a corresponding modulated signal,

demodulation means for converting the modulated signal to a bit string of bits having a first or second logical value, which bit string contains a series of n-bit code words which correspond to the information signal portions, and

converting means for converting the series of code words to the series of information words, an information word being assigned to each of the code words to be converted and depending thereon, in which the converting means convert a code word to an information word also depending on another code word adjacent to the code word being converted, the information signal portions from the at least one group of the first type end in s bit cells having a same logical value, the information signal portions from the at least

one group of the second type end in t bit cells having a same logical value, in which s and t can assume different values and the values that s can assume are different than all the values that t can assume, and t is greater than or equal to 2 and smaller than or equal to 5.

98. (new) An encoding device, comprising an m-to-n bit converter for converting m-bit information words to n-bit code words, means for converting the n-bit code words to a modulated signal, and state establishing means for establishing a coding state on the delivery of a code word by the converter, the state establishing means being arranged for establishing a first type of coding state for each delivered code word belonging to a group of a first type, which state is determined only by the group to which the delivered code word belongs, and for establishing a second type of coding state for each of the delivered code words belonging to a group of the second type, which state is determined not only by the group to which the delivered code word belongs but also by information content in the information word converted into the delivered code word, in which the m-to-n bit converter comprises means for selecting a code word corresponding to an information word from a set of code words, the set corresponding respectively to the established coding state of the first type or the second type, sets of code words belonging to coding states of the second type containing no code words in common with other sets of code words belonging to coding states of the second type, in which at least one of the sets of code words for each of at least a number of information words comprise at least a pair of code words, with low-frequency components in the modulated signal being repressed when the information words are converted by selection of code words from the pairs of code words.

99. (new) A device for recording information, which device comprises a coding device of claim 98 for converting a series of information words representing the information to a modulated signal, and means for recording on a record carrier an information

pattern corresponding to the signal.

100. (new) A record carrier having a signal recorded in a track, the signal comprising a sequence of successive information signal portions, each signal portion representing an information word in which each of the information signal portions comprises n bit cells having a first or second logical value and in which a plurality of track information patterns represent the information signal portions, and in which the information signal portions are spread over at least one group of a first type and at least one group of a second type, while each information signal portion belonging to a group of the first type uniquely represents an information word and each information signal portion belonging to a group of the second type in combination with the logical values of p bit cells at predetermined non-consecutive positions in a following signal portion represent a unique information word, thereby allowing one information signal portion belonging to the at least one group of the second type to represent a plurality of information words among which the respective information word is distinguishable, in which at least one of the sets of code words for each of at least a number of information words comprise at least a pair of code words, with low-frequency components in the modulated signal being repressed when the information words are converted by selection of code words from the pairs of code words.

101. (new) A modulated signal representing a series of information words for subsequent reading, demodulation and decoding to reproduce the represented series of information words, the coded signal comprising a sequence of q successive information signal portions which represent q information words, where q is an integer, in which signal each of the information signal portions represents one of the information words and comprises n bit cells, each the bit cell having a first or second logical value, each information signal portion belonging to one of a plurality of predetermined groups of information signal portions, each information signal portion belonging to a first one of the groups

of information signal portions uniquely establishing an information word irrespective of information signal portions adjacent to the each information signal portion belonging to the first group, and each information signal portion belonging to a second one of the groups of information signal portions uniquely establishing an information word depending upon the logical values of p bit cells at predetermined non-consecutive positions in a signal portion adjacent to the each information signal portion belonging to the second group, in which at least one of the sets of code words for each of at least a number of information words comprise at least a pair of code words, with low-frequency components in the modulated signal being repressed when the information words are converted by selection of code words from the pairs of code words.

102. (new) A decoding device for converting a modulated signal to a series of m-bit information words, the device comprising:

demodulation means for converting the modulated signal to a bit string of bits having a first or second logical value, which bit string contains a series of n-bit code words which correspond to the information signal portions, and

converting means for converting the series of code words to the series of information words, an information word being assigned to each of the code words to be converted and depending thereon, in which the converting means convert a code word to an information word also depending on another portion of the bit stream adjacent to the code word being converted if the information signal portions end in t bit cells having a same logical value, and not if the information signal portions end in s bit cells having a same logical value, where s and t can assume different values, the values that s can assume are all different than the values that t can assume, and t is greater than or equal to 2 and smaller than or equal to 5, in which at least one of the sets of code words for each of at least a number of information words comprise at least a pair of code words, with low-frequency components in the modulated signal being repressed when the information words are converted by selection of code words from the pairs of code words.

103. (new) A reading device for reading a record carrier on which information is recorded in an information pattern, the device comprising:

reading means for converting the information pattern to a corresponding modulated signal,

demodulation means for converting the modulated signal to a bit string of bits having a first or second logical value, which bit string contains a series of n-bit code words which correspond to the information signal portions, and

converting means for converting the series of code words to the series of information words, an information word being assigned to each of the code words to be converted and depending thereon, in which the converting means convert a code word to an information word also depending on another portion of the bit stream adjacent to the code word being converted if the information signal portions end in t bit cells having a same logical value, and not if the information signal portions end in s bit cells having a same logical value, where s and t can assume different values, the values that s can assume are all different than the values that t can assume, and t is greater than or equal to 2 and smaller than or equal to 5, in which at least one of the sets of code words for each of at least a number of information words comprise at least a pair of code words, with low-frequency components in the modulated signal being repressed when the information words are converted by selection of code words from the pairs of code words.

104. (new) A record carrier having a signal recorded in a track, the signal comprising a sequence of successive information signal portions, each information signal portion representing an information word in which each of the information signal portions comprises n bit cells having a first or second logical value and in which a plurality of track information patterns represent the signal portions, and in which the information signal portions are spread over at least one group of a first type and at least one group of a second type, while each information signal portion

belonging to a group of the first type uniquely represents an information word and each information signal portion belonging to a group of the second type in combination with the logical values of p bit cells at the same predetermined non-consecutive positions in a respective immediately following signal portion represent a unique information word, where p is an integer smaller than n, and in which low frequency components of the modulated signal are repressed.

105. (new) A decoding device for converting a modulated signal to a series of m-bit information words, the device comprising:

demodulation means for converting the modulated signal to a bit string of bits having a first or second logical value, which bit string contains a series of n-bit code words which correspond to information signal portions, and

converting means for converting the series of code words to the series of information words, an information word being assigned to each of the code words to be converted and depending thereon, in which the converting means convert a code word to an information word also depending on the logical values of bits at p predetermined non-consecutive bit positions in an adjacent portion of the bit string, where p is an integer smaller than n, and in which low frequency components of the modulated signal are repressed.

106. (new) A reading device for reading a record carrier on which information is recorded in an information pattern, the device comprising:

means for converting the information pattern to a corresponding modulated signal,

demodulation means for converting the modulated signal to a bit string of bits having a first or second logical value, which bit string contains a series of n-bit code words which correspond to the information signal portions, and

converting means for converting the series of code words to the series of information words, an information word being assigned

to each of the code words to be converted and depending thereon, in which the converting means convert a code word to an information word also depending on the logical values of bits at p predetermined non-consecutive bit positions in the adjacent portion of the bit string, where p is an integer smaller than n, and in which the low frequency components of the modulated signal are repressed.

107. (new) The carrier of claim 2, in which the positions of the p bit cells are spaced at least d apart.

108. (new) The carrier of claim 18, in which the positions of the p bit cells are spaced at least d apart both within information signal portions and across information signal portion boundaries.

109. (new) The method of claim 25, in which the information in the information word that determines the coding state is the logical value of p bits of the information word and the positions of the p bits are spaced at least d apart both within information signal portions and across information signal portion boundaries

110. (new) The device of claim 37, in which the p bit positions are spaced at least d apart both within information signal portions and across information signal portion boundaries.

111. (new) The carrier of claim 46, in which the positions of the p bit cells are spaced at least d apart both within information signal portions and across information signal portion boundaries.

112. (new) The device of claim 55, in which the positions of the p bit cells are spaced at least d apart both within information signal portions and across information signal portion boundaries.

113. (new) A signal produced by the method of claim 22.

114. (new) A record carrier comprising the signal produced by the

method of claim 22.

115. (new) A record carrier comprising the signal produced by the method of claim 92.

116. (new) A device for recording information, which device comprises a coding device of claim 33 for converting a series of information words representing the information to a modulated signal, and means for recording on a record carrier an information pattern corresponding to the signal.

117. (new) An encoder comprising:

an input for receiving successive information words, each information word having an information word value,

means for converting the information words into corresponding information signal portions,

means for providing sync signal portions, and

output means for supplying successive signal portions, the successive signal portions including the information signal portions and the sync signal portions, each successive signal portion containing multiple bit cell positions, each bit cell position having a signal value selected between a first signal value and a different second signal value, a bit cell pattern for each signal portion depending on the signal values of the bit cell positions, the information signal portions containing n bit cell positions, and wherein:

the bit cell patterns of the information signal portions are logically organizable into multiple groups of bit cell patterns, the groups including at least one group of a first type and at least one group of a second type,

each bit cell pattern that belongs to a group of the first type represents a single information word value,

each bit cell pattern that belongs to a group of the second type represents multiple different information word values,

the bit cell pattern of each information signal portion having a bit cell pattern belonging to a group of the second type, in

combination with a sub bit cell pattern, depending on the signal values at p predetermined bit cell positions in an immediately following adjacent signal portion, represents a single information word value, where p is less than n,

the sync signal portions are between series of q successive information signal portions in the successive signal portions, the sync signal portions having bit cell patterns that do not occur within the series of q successive information signal portions, the sync signal portions including multiple different sync signal portions in which the values at some bit cell positions are mutually the same and the signal values at other bit cell positions are mutually different,

the adjacent signal portions immediately following the information signal portions having bit cell patterns belonging to a group of the second type being in some cases an adjacent information signal portion containing the p bit cell positions and being in other cases an adjacent sync signal portion containing the p bit cell positions.

118. (new) A recorder comprising:

the encoder of claim 117 for supplying the successive signal portions from the information words, and

means for forming a pattern of detectable differences in properties of the record carrier along a track of the record carrier to represent the successive signal portions.

119. (new) A method of producing record carriers, comprising:

receiving successive information words, each information word having an information word value,

converting the information words into corresponding information signal portions,

providing sync signal portions; and

outputting successive signal portions including the information signal portions and the sync signal portions, each signal portion containing multiple bit cell positions, each bit cell position having a signal value selected between different

first and second values, the signal values of the bit cell positions of the signal portions defining bit cell patterns, the information signal portions having n bit cell positions, and

forming record carriers having detectable difference in properties alternating along a track, the differences in properties represents the first and second signal values of the bit cell positions of the successive signal portions, and wherein:

the bit cell patterns being logically organizable into multiple groups of bit cell patterns, the groups including at least one group of a first type and at least one group of a second type,

each bit cell pattern that belongs to a group of the first type uniquely represents an information word value,

each bit cell pattern that belongs to a group of the second type represents multiple different information word values,

the bit cell pattern of each information signal portion having a bit cell pattern belonging to a group of the second type, in combination with a sub bit cell pattern depending on the signal values at p predetermined bit cell positions in an immediately following adjacent signal portion in the successive signal portions, represents a single information word value,

the sync signal portions are provided between series of q successive information signal portions in the successive signal portions, the sync signal portions having bit cell patterns that do not occur within the series of q successive information signal portions, the sync signal portions including different sync signal portions in which the values at some bit cell positions are mutually the same and the signal values at other bit cell positions are mutually different,

the adjacent signal portions immediately following the information signal portions having bit cell patterns belonging to a group of the second type in some cases being an adjacent information signal portion containing the p bit cell positions and in other cases being an adjacent sync signal portion containing the p bit cell positions.

120. (new) A decoder comprising:

an input for receiving successive signal portions, each signal portion represents multiple bit cell positions having a first or different second signal value defining a bit cell pattern of the signal portion, the signal portions including sync signal portions and information signal portions having n bit cell positions,

means for converting the information signal portions into corresponding information words, each information word having an information word value, and

an output for supplying the information words, and wherein:

the bit cell patterns of the information signal portions are logically organizable into multiple groups of bit patterns, the groups including at least one group of a first type and at least one group of a second type,

each bit pattern belonging to a group of the first type represents a single information word value,

each bit cell pattern that belongs to a group of the second type represents multiple different information word values,

the bit cell pattern of each information signal portion having a bit cell pattern belonging to a group of the second type, in combination with a sub bit cell pattern depending on the signal values at p predetermined bit cell positions in an immediately following adjacent signal portion, represents a single information word value,

the sync signal portions being between groups of q successive information signal portions in the sequential signal portions, the sync signal portions having bit cell patterns that do not occur in the q successive information signal portions, the sync signal portions including different sync signal portions in which the values at some bit cell positions are mutually the same and the signal values at other bit cell positions are mutually different,

the adjacent signal portions immediately following the information signal portions having bit cell patterns belonging to a group of the second type in some cases being an adjacent information signal portion containing the p bit cell positions and in other cases being an adjacent sync signal portion containing the p bit cell positions.

121. (new) A player comprising:

means for reading successive signal portions from a record carrier, and

the decoder of claim 120 for supplying successive information words from the decoded information signal portions of the successive signal portions.

122. (new) A method of providing information, comprising:

receiving successive signal portions, each signal portion comprising multiple bit cell positions, each bit cell position having a signal value selected from different first and second signal values defining a bit cell pattern, the signal portions including sync signal portions and information signal portions having n bit cell positions,

means for converting the information signal portions into corresponding information words, each information word having an information word value, and

an output for supplying information words, and wherein:

the bit cell patterns of the information signal portions are logically organizable into multiple groups of bit cell patterns, the groups including at least one group of a first type and at least one group of a second type,

each bit cell pattern that belongs to a group of the first type represents a single information word value,

each bit cell pattern that belongs to a group of the second type represents multiple different information word values,

the bit cell pattern of each information signal portion having a bit cell pattern belonging to a group of the second type, in combination with a sub bit cell pattern depending on the signal values at p predetermined bit cell positions in an immediately following adjacent signal portion, represents a single information word value,

the sync signal portions separating groups of q successive information signal portions, the sync signal portions having bit cell patterns that do not occur in the q successive information

signal portions, the sync signal portions including different sync signal portions in which the values at some bit cell positions are mutually the same and the signal values at other bit cell positions are mutually different,

the adjacent signal portions immediately following the information signal portions having bit cell patterns belonging to a group of the second type in some cases being an adjacent information signal portion containing the p bit cell positions and in other cases being an adjacent sync signal portion containing the p bit cell positions.

123. (new) A signal in a medium, comprising a sequence of successive signal portions including information signal portions and sync signal portions, each successive signal portion containing multiple bit cell positions, each bit cell position having a signal value selected between different first and second signal values, a bit cell pattern for each signal portion depending on the signal values of the bit cell positions, the information signal portions containing n bit cell positions, the information signal portions being decodable into useful information words, and wherein:

the bit cell patterns of the information signal portions are logically organizable into multiple groups of bit cell patterns, the groups including at least one group of a first type and at least one group of a second type,

each bit cell pattern that belongs to a group of the first type represents a single information word value,

each bit cell pattern that belongs to a group of the second type represents multiple different information word values,

the bit cell pattern of each information signal portion having a bit cell pattern belonging to a group of the second type, in combination with a sub bit cell pattern depending on the signal values at p predetermined bit cell positions in an immediately following adjacent signal portion, represents a single information word value,

the sync signal portions separating series of q successive information signal portions in the successive signal portions, the

sync signal portions having bit cell patterns that do not occur within the series of q successive information signal portions, the sync signal portions including different sync signal portions in which the values at some bit cell positions are mutually the same and the signal values at other bit cell positions are mutually different,

the adjacent signal portions immediately following the information signal portions having bit cell patterns belonging to a group of the second type in some cases being an adjacent information signal portion containing the p bit cell positions and in other cases being an adjacent sync signal portion containing the p bit cell positions.

124. (canceled)

125. (new) A record carrier having a signal recorded in a track, the signal comprising a sequence of successive signal portions including information signal portions and sync signal portions, each successive signal portion containing multiple bit cell positions, each bit cell position having a signal value selected between different first and second signal values, a bit cell pattern for each signal portion depending on the signal values of the bit cell positions, the information signal portions containing n bit cell positions, the information signal portions being decodable into useful information words, and wherein:

the bit cell patterns of the information signal portions are logically organizable into multiple groups of bit cell patterns, the groups including at least one group of a first type and at least one group of a second type,

each bit cell pattern that belongs to a group of the first type represents a single information word value,

each bit cell pattern that belongs to a group of the second type represents multiple different information word values,

the bit cell pattern of each information signal portion having a bit cell pattern belonging to a group of the second type, in combination with a sub bit cell pattern depending on the signal

values at p predetermined bit cell positions in an immediately following adjacent signal portion, represents a single information word value,

the sync signal portions separating series of q successive information signal portions in the successive signal portions, the sync signal portions having bit cell patterns that do not occur within the series of q successive information signal portions, the sync signal portions including different sync signal portions in which the values at some bit cell positions are mutually the same and the signal values at other bit cell positions are mutually different,

the adjacent signal portions immediately following the information signal portions having bit cell patterns belonging to a group of the second type in some cases being an adjacent information signal portion containing the p bit cell positions and in other cases being an adjacent sync signal portion containing the p bit cell positions.

126. (new) The record carrier of claim 1 wherein the sync signal portions include sync signal portions that are mutually different and have the same 22-bit ending portions.

127. (new) The method of converting of claim 86 wherein the sync signal portions include sync signal portions that are mutually different and have the same 22-bit ending portions.

128. (new) The encoding device of claim 87 wherein the sync signal portions include sync signal portions that are mutually different and have the same 22-bit ending portions.

129. (new) The coded signal of claim 89 wherein the sync signal portions include sync signal portions that are mutually different and have the same 22-bit ending portions.

130. (new) The decoding device of claim 90 wherein the sync signal portions include sync signal portions that are mutually different

and have the same 22-bit ending portions.

131. A coding device comprising:

an input for receiving a sequence of m-bit information words;

a memory that stores (n+s) values and that delivers a corresponding (n+s) parallel binary output signal of one of the (n+s) values in response to each reception of an (m+s+i) parallel binary input signal, the same (m+s+i) input signal value always results in the delivery of the same corresponding (n+s) output signal value, the memory being connected to the input for receiving the m information words as the m input signals, bits of the stored (n+s) values have a logical consecutive bit order, the (n+s) values stored in the memory being arranged so that: for most (m+s) input values, the same (n+s) output value is always delivered for the same (m+s) input value and a different (n+s) output value is delivered for each different (m+s) input value; at different times, for some (m+s) input values, the memory delivers a different one of two different (n+s) output values for the same (m+s) input value; the value of the i binary input signal selects between the two different (n+s) output values for the same (m+s) input value; at different times, different first and second values of the m input signals result in the same values of the corresponding n output signals and result in different respective first and second values of the s output signals; the same p predetermined non-consecutive bits always have different values in the stored n values corresponding to s input signals corresponding to said different respective first and second values of the s output signals;

a first buffer memory with an input connected to store the s parallel binary output signals and an output connected to provide the stored signals as s parallel binary input signals to the memory;

a parallel-to-serial converter that converts each n-bit parallel binary output signal into a corresponding serial n-bit code word of consecutive bits, the logical bit order of the n-bit values stored in the memory corresponding to the bit order in the serial n-bit code words;

a second buffer memory for storing a sum of the differences between a number of first binary values and a number of second binary values of the code words;

an arithmetic circuit that determines a new sum of the differences by combining the sum of the differences previously stored in the second buffer memory with the difference between the number of first binary values and the number of second binary values of the code words, and that stores the new sum of the differences in the second buffer memory; and

a detecting circuit for providing the i binary input signal depending on the sum of the differences, the i input signal suppressing the sum of the differences between the number of first binary values and the number of second binary values of the n parallel binary output signals

an output that delivers sequential words including sequences of the code words.

132. (new) The coding device of claim 131, wherein the memory includes a ROM module.

133. (new) The coding device of claim 131, wherein the memory includes a combinatorial logical circuit formed by gate circuits and synchronized by clock signals.

134. (new) The coding device of claim 131, further comprising a modulo-2 integrator for modulating the words before they are delivered by the output and wherein the number of first and second binary values are determined from the code words after they are modulated.

135. (new) The coding device of claim 131, wherein the memory also stores multiple different sync word values and deliver parallel sync words of one of the synch word values in response to a count of the code words, the value of the delivered synch word depending on the s input signals, the value of the sync words being different

than the value of any portion of the delivered sequence of words and code words of the same length as the code words.

136. (new) The coding device of claim 131, further comprising:

a third buffer memory containing different sync words and delivering one of the sync words depending on a count signal and the s input signals, the same sync code only resulting from the same s values, the value of the sync words being different than the value of any portion of the delivered sequence of words and code words of the same length as the code words;

a switch connected to toggle between: delivering the code words from the parallel to serial converter; and delivering a sync word from the third buffer in response to the count signal;

a counter that counts the delivered code words in a series of multiple code words and generates the count signal to insert a sync word after each series of a predetermined number of code words.

137. (new) The coding device of claim 136, wherein the sync words are stored in the third buffer memory such that the same p non-consecutive bits always have different values in the sync words corresponding to s input signals corresponding to the different respective first and second values of the s output signals.

138. (new) The coding device of claim 136, wherein the same p predetermined non-consecutive bits are bits 1 and 13 and the ending portions following bit 13 of all the sync words have the same value.

139. (new) The coding device of claim 131, wherein the memory stores (n+s+t) values and delivers a corresponding (n+s+t) parallel binary output signal of one of the (n+s+t) values, the same (m+s+i) input signal value always resulting in the delivery of the same corresponding (n+s+t) output signal value, t being a t-bit output signal, one or more, the t values indicating one or more of:

whether different n output values are output for the same m input value;

the difference between the number of first binary values and the number of second binary values of the n output values;

the difference between the number of first binary values and the number of second binary values of each of the n output values for the same m input values;

whether the number of first binary values is even or odd for the n output values; and

whether the number of first binary values is even or odd for each of the n output values for the same m input values.

140. (new) The coding device of claim 131, wherein the arithmetic circuit determines a new sum of the differences for each code word resulting from the two different (n+s) output values for the same m+s input value, the detection circuit provides the i input signal selecting between the two n+s output values for suppressing the sum of the differences, and the coding device further comprising a multiplexer for storing one of the two determined new sum of the differences in the second buffer memory depending on the i input signal.

141. (new) A decoding device comprising:

an input for receiving consecutive words including n-bit code words;

a memory that stores m-bit information word values and that outputs m-bit information words in response to receiving an n-bit code word and at times also in response to values of the same p predetermined non-consecutive bits of the next consecutive word, the same value of the code word combined with the same values at the same p predetermined non-consecutive bit positions of the next word always resulting in the delivery of the same information word whereby the m-bit information word output for each respective n-bit code word being independent of all code words previous to the respective n-bit code word, the information word values stored in the memory being arranged for retrieval so that: at times the value of the delivered information word depends on the values of the p non-consecutive bits of the next consecutive word and at other

times the delivered information word is independent of the value of the p non-consecutive bits of the next consecutive word; at different times the same information word value is delivered in response to different respective code word values that follow respective preceding code words wherein the respective preceding code words mutually have the same value.

142. (new) The decoding device of claim 141, further comprising:
a modulo-2 differentiator for demodulating the received words.

143. (new) The decoding device of claim 141, further comprising:
a shift register that stores at least portions of received words and that provides the n-bit code word and p non-consecutive bits of the next word to the memory;
a sync word detector for detecting a sync word in the shift register;
a synchronizer that shifts the shift register in response to the detection of the sync word and that signals the memory to output an information word when the code word and the same p predetermined non-consecutive bits of the next word are correctly shifted into the shift register.

144. (new) The decoding device of claim 141, wherein at times the next consecutive word after a code word is a sync word containing the same p predetermined non-consecutive bits.

145. (new) The decoding device of claim 141, wherein the information word values stored in the memory are arranged for retrieval so that: when the value of the delivered information word also depends on the value of the same p predetermined non-consecutive bits of the next code word, then the code word ends in s bits having the same value; and when the value of the delivered information word is independent of the value of the same p predetermined non-consecutive bits of the next word, then the code word ends in t bits having the same value; and wherein s can assume different values and t can assume different values and the values

that s can assume are all different than the values that t can assume.